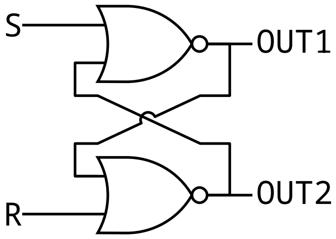
Worksheet: SR Latch

SR Latch (Set-Reset Latch)



Examine the logic diagram of an SR latch to the left. If you try to write a truth table for this circuit, your mind may get caught in a loop. The output not only depends on the inputs are set to, but there is also a feedback loop from the outputs back into gate inputs.

To analyze this, let us make an initial assumption. Let us set S and R both to 0 and <u>assume</u> the initial value of OUT1 is also 0. Then it is easy to determine that OUT2, which is equal to $\overline{\text{OUT1} \lor \text{R}}$, will evaluate to 1. Similarly, if S and R are both 0 and OUT1 is assumed to be 1, then OUT2 will evaluate to 0. Write these values in the table to the right.

S	R	OUT1	OUT2
0	0	0	
0	0	1	

Let us verify that this state is stable. If S and R are both set to 0 and we <u>assume</u> that OUT2 is 0, what will the state of OUT1 be? Since $\text{OUT1} = \overline{\text{OUT2} \lor \text{S}}$, the value of OUT1 will evaluate to 1. And again, if OUT2 is assumed to be 1, this expression will evaluate to 0. Write these values in the table to the right.

S	R	OUT1	OUT2
0	0		1
0	0		0

The above analysis shows that when S and R are both set to 0, the circuit is stable, and although we do not know the state of OUT1 or OUT2, we do know that OUT1 is always the inverse of OUT2.

Fill out the table below. We start with both S and R set to 0, and OUT1 the inverse of OUT2. The value of S is then changed to 1. Given the values of S and R, and the initial values of OUT1 and OUT2, calculate what the values of OUT1 and OUT2 will change to.

Notice for the second row, we have a state where OUT1 and OUT2 are the same. But we learned from the above analysis that this state is not stable. So, using $\text{S} = 1$ and $\text{R} = 0$, and the *intermediate* values of OUT1 and OUT2, calculate the final values for OUT1 and OUT2.

S	R	OUT1	OUT2
0	0	0	1
0	0	1	0

→

		initial		**intermediate**		**final**	
S	**R**	**OUT1**	**OUT2**	**OUT1**	**OUT2**	**OUT1**	**OUT2**
1	0	0	1				
1	0	1	0				

Starting with both S and R set to 0, and an unknown state of OUT1 and OUT2, if we set S to 1, the end result is OUT1 and OUT2 become determined, with OUT1 set to 0 and OUT2 set to 1.

S	R	OUT1	OUT2
1	0	0	1
1	0	0	1

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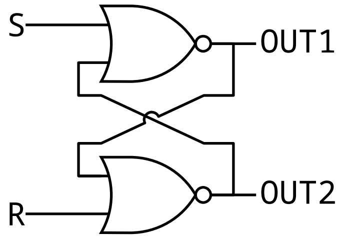


The SR latch circuit is repeated here to the right. Let us perform a similar analysis as above, leaving S set to 0 and changing R to 1.

The intermediate state in this situation becomes unstable in the first row. Using S = 0 and R = 1 , and the *intermediate* values of OUT1 and OUT2, calculate the final values for OUT1 and OUT2.

S	R	OUT1	OUT2
0	0	0	1
0	0	1	0

→

		initial		intermediate		final	
S	**R**	**OUT1**	**OUT2**	**OUT1**	**OUT2**	**OUT1**	**OUT2**
0	1	0	1				
0	1	1	0				

Starting with both S and R set to 0, and an unknown state of OUT1 and OUT2, if we set R to 1, the end result is OUT1 and OUT2 become determined, with OUT1 set to 1 and OUT2 set to 0.

S	R	OUT1	OUT2
0	1	1	0
0	1	1	0

After setting either S to 1 or R to 1, if we thereafter set them back to 0, the value of OUT1 and OUT2 remain determined. Thus we can store a value in this circuit. If we wish to:

- (OUT1, OUT2) to equal (0, 1), we set S to 1
- (OUT1, OUT2) to equal (1, 0), we set R to 1.

There is another situation we have not yet analyzed – setting both S and R to 1.
Complete the table below.

S	R	OUT1	OUT2
0	0	0	1
0	0	1	0

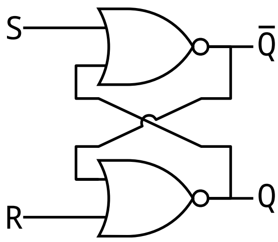
→

		initial		intermediate		final…?	
S	**R**	**OUT1**	**OUT2**	**OUT1**	**OUT2**	**OUT1**	**OUT2**
1	1	0	1				
1	1	1	0				

Notice that the outputs are not in a stable state. If either of S or R is set to 0, then the state can be resolved with the resulting values based on which value, S or R, remains at 1.

However, if both S and R are changed from 1 to 0 at the same time, the final value of OUT1 and OUT2 become unknown.

The final truth table for the SR Latch is given to the right. The names of the outputs have been changed to the more common names: Q and $\overline{Q}$. A value of 1 on the S pin will set Q to 1 while a value of 1 on the R pin will reset Q to 0. The value of $\overline{Q}$ is always opposite that of Q . The behavior of setting both S and R to 1 is undefined.



S	R	$\overline{Q}$	Q
0	0	$\overline{Q}$	Q
1	0	0	1
0	1	1	0
1	1	not permitted	